WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of transistor cells divided and arranged in a plurality of blocks, for forming a bipolar transistor device;

a plurality of first lines provided for said plurality of blocks, respectively, and each electrically coupled with a base region of each said transistor cell of a corresponding one of said blocks;

a plurality of second lines provided for said plurality of blocks, respectively, and each electrically coupled with one of collector and emitter regions of each said transistor cell of a corresponding one of said blocks;

a reference voltage line electrically coupled with the other of said collector and emitter regions of each of said plurality of transistor cells; and

a plurality of bias current supply circuits provided for said plurality of blocks, respectively, and each supplying a bias current to a corresponding one of said plurality of first lines, each said bias current supply circuit decreasing an amount of said bias current to be supplied, when said bias current has increased.

2. The semiconductor device according to claim 1, wherein each said bias current supply circuit includes:

a bias control transistor having a base region receiving a predetermined level of control voltage, electrically coupled between a power supply voltage for generating said bias current and a node supplying said bias current; and

a bias adjusting portion provided to reduce a current drivability of said bias control transistor as said bias current increases.

3. The semiconductor device according to claim 2, further comprising a plurality of radio-frequency attenuation portions provided for said plurality of blocks, respectively, and each electrically coupled between said node corresponding thereto and a corresponding one of said plurality of first lines, to attenuate a radio-frequency component of set bias current.

4. The semiconductor device according to claim 1, further comprising a plurality of ballast resistors provided for said plurality of blocks, respectively, and each electrically coupled between a corresponding one of said plurality of bias supply circuits and a corresponding one of said plurality of first lines, each said bias current supply circuit including a bias control transistor having a base region receiving a predetermined level of control voltage, electrically coupled between a power supply voltage for generating said bias current and a corresponding one of said plurality of ballast resistors.

5. The semiconductor device according to claim 1, further comprising a plurality of feedback circuits provided for said plurality of blocks, respectively, and each electrically coupling a corresponding one of a plurality of second lines and a predetermined internal node together if the corresponding one of said second lines and said internal node have therebetween a voltage difference exceeding a predetermined level of voltage.

6. A semiconductor device comprising:

a plurality of transistor cells divided and arranged in a plurality of blocks, for forming a bipolar transistor device;

a plurality of first lines provided for said plurality of blocks, respectively, and each electrically coupled with a base region of each said transistor cell of a corresponding one of said blocks;

a plurality of second lines provided for said plurality of blocks, respectively, and each electrically coupled with one of collector and emitter regions of each said transistor cell of a corresponding one of said blocks;

a reference voltage line electrically coupled with the other of said collector and emitter regions of each of said plurality of transistor cells; and

a plurality of feedback circuits provided for said plurality of blocks, respectively, and each electrically coupling a corresponding one of a plurality of second lines and a predetermined internal node together if the corresponding one of said second lines and said internal node have

therebetween a voltage difference exceeding a predetermined level of voltage.

7. The semiconductor device according to claim 6, wherein:

said plurality of feedback circuits each include a feedback transistor electrically coupled between said corresponding second line and said internal node, and a voltage adjustment portion referring to a voltage difference between said corresponding second line and said internal node to set a voltage difference between said internal node and a base region of said feedback transistor, each said feedback circuit being arranged in a corresponding one of said blocks at a location experiencing a relatively large heat elevation in operation.

8. The semiconductor device according to claim 7, wherein each said feedback circuit is arranged in a corresponding one of said blocks at a location close to a center of said block.

9. The semiconductor device according to claim 6, further comprising:

a bias supply circuit shared by said plurality of blocks and supplying each of said plurality of first lines with a bias current; and

a plurality of ballast resistors provided for said plurality of blocks, respectively, and each electrically coupled between said bias supply circuit and a corresponding one of said plurality of first lines.

10. A semiconductor device provided on a semiconductor chip, comprising a plurality of bipolar transistor devices for amplifying a signal in phases, of said plurality of bipolar transistor devices said bipolar transistor device of a preceding stage being arranged on said semiconductor chip at a location experiencing a larger temperature elevation than said bipolar transistors of any other subsequent stages.

11. The semiconductor device according to claim 10, wherein:

of said plurality of bipolar transistor devices said bipolar transistor device of a preceding stage is arranged on said semiconductor chip closer to a center area than said bipolar transistors of any other subsequent stages.

12. The semiconductor device according to claim 10, wherein of said plurality of bipolar transistor devices at least one bipolar transistor device including a final stage each includes:

a plurality of transistor cells divided and arranged in a plurality of blocks, for forming said bipolar transistor device;

a plurality of first lines provided for said plurality of blocks, respectively, and each electrically coupled with a base region of each said transistor cell of a corresponding one of said blocks;

a plurality of second lines provided for said plurality of blocks, respectively, and each electrically coupled with one of collector and emitter regions of each said transistor cell of a corresponding one of said blocks;

a reference voltage line electrically coupled with the other of said collector and emitter regions of each of said plurality of transistor cells; and

a plurality of bias current supply circuits provided for said plurality of blocks, respectively, and each supplying a bias current to a corresponding one of said plurality of first lines, each said bias current supply circuit decreasing an amount of said bias current to be supplied, when said bias current has increased.

13. The semiconductor device according to claim 12, wherein:

said at least one bipolar transistor device each further includes a plurality of radio-frequency attenuation portions provided for said plurality of blocks, respectively, and each electrically coupled between a corresponding one of said plurality of bias supply circuits and a corresponding one of said plurality of first lines, to attenuate a radio-frequency component of set bias current; and

each said bias current supply circuit has

a bias control transistor having a base region receiving a predetermined level of control voltage, electrically coupled between a power

supply voltage for generating said bias current and a corresponding one of a plurality of radio-frequency attenuation portions, and

a bias adjusting portion provided to reduce a current drivability of said bias control transistor as said bias current increases.

14. The semiconductor device according to claim 12, wherein said at least one bipolar transistor device each further includes a plurality of ballast resistors provided for said plurality of blocks, respectively, and each electrically coupled between a corresponding one of said plurality of bias supply circuits and a corresponding one of said plurality of first lines, each said bias current supply circuit having a bias control transistor with a base region receiving a predetermined level of control voltage, electrically coupled between a power supply voltage for generating said bias current and a corresponding one of said plurality of ballast resistors.

15. The semiconductor device according to claim 12, wherein said at least one bipolar transistor device each further includes a plurality of feedback circuits provided for said plurality of blocks, respectively, and each electrically coupling a corresponding one of a plurality of second lines and a predetermined internal node together if the corresponding one of said second lines and said internal node have therebetween a voltage difference exceeding a predetermined level of voltage.

16. The semiconductor device according to claim 10, wherein of said plurality of bipolar transistor devices at least one said bipolar transistor device including said final stage each includes:

a plurality of transistor cells divided and arranged in a plurality of blocks, for forming said at least one bipolar transistor device;

a plurality of first lines provided for said plurality of blocks, respectively, and each electrically coupled with a base region of each said transistor cell of a corresponding one of said blocks;

a plurality of second lines provided for said plurality of blocks, respectively, and each electrically coupled with one of collector and emitter

regions of each said transistor cell of a corresponding one of said blocks;

a reference voltage line electrically coupled with the other of said collector and emitter regions of each of said plurality of transistor cells; and

a plurality of feedback circuits provided for said plurality of blocks, respectively, and each electrically coupling a corresponding one of a plurality of second lines and a predetermined internal node together if the corresponding one of said second lines and said internal node have therebetween a voltage difference exceeding a predetermined level of voltage.

17. The semiconductor device according to claim 16, wherein said at least one bipolar transistor device each further includes:

a bias supply circuit shared by said plurality of blocks and supplying each of said plurality of first lines with a bias current; and

a plurality of ballast resistors provided for said plurality of blocks, respectively, and each electrically coupled between said bias supply circuit and a corresponding one of said plurality of first lines.

18. The semiconductor device according to claim 10, wherein of said plurality of bipolar transistors at least one bipolar transistor device including said final stage each includes:

a plurality of transistor cells divided and arranged in a plurality of blocks, for forming said at least one bipolar transistor device;

a plurality of first lines provided for said plurality of blocks, respectively, and each electrically coupled with a base region of each said transistor cell of a corresponding one of said blocks;

a plurality of second lines provided for said plurality of blocks, respectively, and each electrically coupled with one of collector and emitter regions of each said transistor cell of a corresponding one of said blocks;

a reference voltage line electrically coupled with the other of said collector and emitter regions of each of said plurality of transistor cells;

a bias supply circuit shared by said plurality of blocks and supplying each of said plurality of first lines with a bias current; and

a plurality of ballast resistors provided for said plurality of blocks, respectively, and each electrically coupled between said bias supply circuit and a corresponding one of said plurality of first lines.

19. A semiconductor device provided on a semiconductor chip, comprising:

a plurality of transistor cells divided and arranged in a plurality of blocks, for forming a bipolar transistor device;

a plurality of first lines provided for said plurality of blocks, respectively, and each electrically coupled with a base region of each said transistor cell of a corresponding one of said blocks;

a plurality of second lines provided for said plurality of blocks, respectively, and each electrically coupled with one of collector and emitter regions of each said transistor cell of a corresponding one of said blocks;

a reference voltage line electrically coupled with the other of said collector and emitter regions of each of said plurality of transistor cells;

a bias supply circuit shared by said plurality of blocks and supplying each of said plurality of first lines with a bias current; and

a plurality of ballast resistors provided for said plurality of blocks, respectively, and each electrically coupled between said bias supply circuit and a corresponding one of said plurality of first lines, said plurality of ballast resistors being arranged on said semiconductor chip at a region experiencing a greater temperature elevation than a region having said plurality of transistor cells arranged therein.

20. The semiconductor device according to claim 19, wherein:

said plurality of blocks arranged in first and second directions in a matrix; and

said plurality of ballast resistors are each arranged at a region located between a corresponding one of said plurality of blocks and another said block adjacent to said corresponding one of said plurality of blocks in said first direction.